**a. Maximum throughput**  
Requested synthesis clock frequency: 101.783MHzBest synthesis options: Speed and high performance goals  
Requested implementation clock frequency: 98.505MHz  
Implementation options: High performance  
Resource utilization after implementation:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 104 | 17,344 | 1% |  | |
| Number of 4 input LUTs | 144 | 17,344 | 1% |  | |
| Number of occupied Slices | 95 | 8,672 | 1% |  | |
| Number of Slices containing only related logic | 95 | 95 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 95 | 0% |  | |
| Total Number of 4 input LUTs | 152 | 17,344 | 1% |  | |
| Number used as logic | 144 |  |  |  | |
| Number used as a route-thru | 8 |  |  |  | |
| Number of bonded IOBs | 140 | 190 | 73% |  | |
| IOB Flip Flops | 33 |  |  |  | |
| Number of BUFGMUXs | 1 | 24 | 4% |  | |
| Number of MULT18X18SIOs | 2 | 28 | 7% |  | |
| Average Fanout of Non-Clock Nets | 3.00 |  |  |  | |

Maximum clock frequency after implementation: 107.215MHz

**b.     Minimum area**Requested synthesis clock frequency: 95.657MHz  
Best synthesis options: Optimization goal as area, high performanceRequested implementation clock frequency: 65.628MHzImplementation options: High place and route effort  
Resource utilization after implementation:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 70 | 17,344 | 1% |  | |
| Number of 4 input LUTs | 143 | 17,344 | 1% |  | |
| Number of occupied Slices | 78 | 8,672 | 1% |  | |
| Number of Slices containing only related logic | 78 | 78 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 78 | 0% |  | |
| Total Number of 4 input LUTs | 153 | 17,344 | 1% |  | |
| Number used as logic | 143 |  |  |  | |
| Number used as a route-thru | 10 |  |  |  | |
| Number of bonded IOBs | 140 | 190 | 73% |  | |
| IOB Flip Flops | 129 |  |  |  | |
| Number of BUFGMUXs | 1 | 24 | 4% |  | |
| Number of MULT18X18SIOs | 2 | 28 | 7% |  | |
| Average Fanout of Non-Clock Nets | 2.61 |  |  |  | |

Maximum clock frequency after implementation: 76.115MHz

**c. Maximum throughput to area ratio**  
Requested synthesis clock frequency: 101.783MHz  
Best synthesis options: Normal optimization effort, with the optimization goal being AreaRequested implementation clock frequency: 98.505MHz  
Implementation options: High Optimization  
Resource utilization after implementation:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Device Utilization Summary** | | | | | **[-]** |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 104 | 17,344 | 1% |  | |
| Number of 4 input LUTs | 144 | 17,344 | 1% |  | |
| Number of occupied Slices | 95 | 8,672 | 1% |  | |
| Number of Slices containing only related logic | 95 | 95 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 95 | 0% |  | |
| Total Number of 4 input LUTs | 152 | 17,344 | 1% |  | |
| Number used as logic | 144 |  |  |  | |
| Number used as a route-thru | 8 |  |  |  | |
| Number of bonded IOBs | 140 | 190 | 73% |  | |
| IOB Flip Flops | 33 |  |  |  | |
| Number of BUFGMUXs | 1 | 24 | 4% |  | |
| Number of MULT18X18SIOs | 2 | 28 | 7% |  | |
| Average Fanout of Non-Clock Nets | 3.00 |  |  |  | |

Maximum clock frequency after implementation: 107.215MHz